--27. A semiconductor integrated circuit device according to claim 25, wherein each of the plurality of memory cells includes a MOS transistor and a capacitor, and wherein said processing circuit is formed by MOS transistors.

--28. A semiconductor integrated circuit device according to claim 26, wherein each of the plurality of memory cells includes a MOS transistor and a capacitor, and said processing circuit is formed by MOS transistors.

--29. A semiconductor integrated circuit device on a semiconductor chip, comprising:

a first memory array including a plurality of DRAM memory cells;

a logic circuit coupled to said first memory array, said logic circuit being formed by MOS transistors;

an input/output circuit coupled to said first memory array, said input/output circuit having nodes to and from which data is input and output outside of said semiconductor chip;

a first signal path coupled between said first memory array and said logic circuit; and